Claims

What is claimed is:

1. A **method** for implementing a **system interconnect** for transporting a **first cell** containing a plurality of **data** between a **plurality of nodes** wherein said system interconnect includes: **a first unidirectional path** between each **pair of adjacent nodes** of said plurality of nodes, said first unidirectional path includes an **incoming end** and an **outgoing end** and a **first plurality of signal lines** and a **frequency reference line**, said pair of adjacent nodes having a **source node** and a **receiver node**, each of said plurality of nodes includes an **input section** connected to said incoming end of an **input path**, and an **output section** connected to said outgoing end of an **output path**, said method comprising steps of:

(a) **providing** a **frequency reference signal** on said frequency reference line to said plurality of nodes;

(b) **generating**, by a **phase lock loop frequency multiplier**, a **node clock** based on said frequency reference signal, said node clock having the same frequency for each of said plurality of nodes, said source node having a **source node clock** and said receiver node having a **receiver node clock**;

(c) **transmitting** said first cell from said output section of said source node to said input section of said receiver node over a **first unidirectional path**, by emitting a plurality of **data transitions** representing said first cell, onto a **first plurality of signal lines** at said outgoing end of said first unidirectional path; and

(d) **receiving** said data transitions from said first plurality of signal lines at said incoming end of said first unidirectional path at said input section of said receiver node.

2. The method of claim 1 wherein said receiver node further comprises an **address comparator mechanism** and a **node address**, said first cell comprises a **destination address**, and said method further comprises:

(e) **comparing** said node address with said destination address.

3. The method of claim 2 wherein said method further comprises:

(f) **emitting** said plurality of data transitions, in synchronization with said receiver node clock, onto a **second plurality of data lines** at said outgoing end of a **second unidirectional path** while receiving said data transitions from said first plurality of signal lines.

4. The method of claim 2 wherein said method further comprises:

(f1) **detecting** that said receiver node is transmitting a **second cell** at said outgoing end of a **second unidirectional path**;

(f2) **storing** a **third cell** in a **bypass buffer** if said node address is different from said destination address, said third cell constructed from said data transitions received at step (d);

(f3) **detecting** when said second cell has been completely transmitted; and

(f4) **transmitting** said third cell from said bypass buffer at said outgoing end of said second unidirectional path.

5. The method of claim 2 wherein said method further comprises:

(f) **swallowing** said plurality of data transitions defining a **second cell** if said node address is the same as said destination address.

6. The method of claim 5 wherein said method further comprises the steps of:

(g) **processing** said second cell; and

(h) **transmitting a response cell** addressed to said source node from said output section of said receiver node.

7. The method of claim 6 wherein step (c) further comprises **storing a copy of said first cell** in a **cell storage**, and further comprising the steps of:

(i) **receiving** said response cell at said source node; and

(j) **removing** said copy of said first cell from said cell storage.

8. The method of claim 2 wherein said first cell is a **broadcast cell**, and further comprising:

(f) **capturing a second cell**; and

(g) **emitting** said plurality of data transitions onto a **second plurality of data lines** at said outgoing end of a **second unidirectional path**.

9. The method of claim 8 further comprising:

(h) processing said second cell; and

(i) transmitting a response cell to said source node.

10. The method of claim 1 further comprising:

initializing each of said nodes by emitting a plurality of **training signal edges** on each of said first plurality of signal lines to condition each of said plurality of DLLs such that said training signal edges are synchronized with said node clock.

11. The method of claim 1 wherein said input section includes a plurality of **adjustable delays** with one adjustable delay for each of said first plurality of signal lines, and further comprising:

synchronizing said data transitions from said first plurality of signal lines to said receiver node clock through use of said plurality of adjustable delays.

12. The method of claim 1 wherein said input section includes an **adjustable delay** and further comprising:

synchronizing said data transitions from said first plurality of signal lines to said receiver node clock through use of said adjustable delay.

13. A **method** for implementing a **system interconnect** for initializing a **plurality of nodes** on a **ring network** having a **plurality of links**, said method comprising steps of:

(a) **emitting** a **reset sequence** from a **first node** to reset a **second node** upon detection of said reset sequence;

(b) **emitting** said reset sequence from said second node; and

(c) **terminating** emission of said reset sequence by said first node upon receipt of said reset sequence at said first node.

14. The method of claim 13 further comprising steps of:

(d) **emitting** a **training sequence** from said first node to train said second node;

(e) **emitting** said training sequence from said second node; and

(f) **terminating** emission of said training sequence by said first node upon detection of said training sequence at said first node.

15. A **method** for implementing a **system interconnect** having a **plurality of nodes**, said interconnect for transporting a **cell** from a **source node** on a **ring network** to a **destination node** on said network, said network having a **first path** and a **second path**, one of said plurality of nodes being a **configuration node**, said method comprising steps of:

(a) **initializing** said plurality of nodes;

(b) **emitting** onto said first path, by said configuration node, a **first identifying address sequence** containing a **configuration node address**;

(c) **receiving** from said first path said first identifying address sequence by a **second node**;

(d) **modifying** said configuration node address contained in said first identifying address sequence to create a **second node address**; and

(e) **emitting** onto said first path, by said second node, a **second identifying address sequence** containing said second node address.

16. The method of claim 15 further comprising steps of:

(b1) **emitting** onto said second path, by said configuration node, said first identifying address sequence containing said configuration node address;

(c1) **receiving** from said second path by said second node a **third identifying address sequence** dependent on said second node's position on said second path;

(f) **determining a number of nodes** on said ring network; and

(g) **initializing a link selection register** (LSR) to indicate which of said first path and said second path is a **preferred path** to each of said plurality of nodes by using information contained in said first identifying address sequence and said third identifying address sequence.

17. A **method** for implementing a **system interconnect** for transporting a **cell** from a **source node** to a **destination node** on a **ring network** having a **plurality of links**, said method comprising steps of:

(a) **detecting** an **interrupt condition change** at said source node, said interrupt condition change comprising either an **interrupt assertion** or an **interrupt deassertion**;

(b) **creating** an **interrupt cell** at said source node responsive to the detecting said interrupt condition change, said interrupt cell being addressed to said destination node and containing said interrupt condition change;

(c) **transporting** said interrupt cell to said destination node; and

(d) **asserting** an **interrupt signal** at said destination node responsive to said interrupt condition change.

18. The method of claim 17 wherein step (d) further comprises:

(d1) **recognizing** said interrupt cell containing said interrupt assertion at said destination node; and

(d2) **incrementing** an **up/down counter**.

19. The method of claim 18 wherein step (d) further comprises:

(d3) **detecting** that said up/down counter is non-zero; and

(d4) **posting** an **interrupt** at said destination node.

20. The method of claim 17 wherein said cell further comprises a **source node identifier** and step (d) further comprises:

(d1) **saving** said source node identifier and said interrupt condition change.

21. The method of claim 17 wherein step (d) further comprises:

(d1) **recognizing** said interrupt cell containing said interrupt deassertion; and

(d2) **decrementing** an **up/down counter**.

22. The method of claim 21 wherein step (d) further comprises:

(d3) **detecting** that said up/down counter is zero; and

(d4) **clearing** an **interrupt** at said destination node.

23. The method of claim 17 wherein said interrupt cell comprises an **interrupt security code** and step (d) further comprises **matching** said interrupt security code with a **destination node interrupt security code**.

24. A **method** for implementing a **system interconnect** for transporting a **cell** from a **source node** to a **destination node** of a **plurality of destination nodes** on a **ring network** having a **plurality of links**, said method comprising steps of:

(a) **tracking** a **number of incomplete transactions**;

(b) **delaying** generation of said cell if one more than said number of incomplete transactions is outside a **sliding window width**;

(c) **generating** said cell after one more than said number of incomplete transactions is within said sliding window width; and

(d) **transporting** said cell to said destination node.

25. The method of claim 24 wherein the tracking said number of incomplete transactions comprises **tracking** one of said number of transactions sent from said source node to said destination node.

26. The method of claim 24 wherein said method further comprises:

(f) **accounting** for an **increase** in said number of incomplete transactions.

27. The method of claim 26 wherein said method further comprises:

(g) **detecting** a **response cell** sent from said destination node;

(h) **completing** an **incomplete transaction** dependent on said response cell; and

(i) **accounting** for a **decrease** in said number of incomplete transactions.

28. The method of claim 24 wherein said destination node is a **hop node**:

29. The method of claim 24 wherein step (a) further comprises:

(a1) **receiving**, by said source node, a **previously sent cell** sent from said source node; and

(a2) **reducing** a **sliding window width**.

30. The method of claim 24 wherein step (a) further comprises:

tracking a **plurality of number of incomplete transactions** sent from said source node to each of said plurality of destination nodes.

31. A **method** for implementing a **system interconnect** for transporting a **cell** from a **source node** to a **destination node** on a **ring network** including a **clockwise path** and a **counterclockwise path**, said method comprising steps of:

(a) **accessing** a **link selection register** at said source node to select which of said clockwise path and said counterclockwise path transports said cell; and

(b) **transporting** said cell to said destination node over said clockwise or counterclockwise path as selected.

32. The method of claim 31 wherein step (a) further comprises:

(a1) **configuring** said link selection register at said source node to specify a **preferred path** to said destination node by specifying which of said clockwise path and said counterclockwise path is used to transport said cell to said destination node.

33. The method of claim 32 wherein said system interconnect includes an **intermediate node** between said source node and said destination node on one of said paths, and step (a) further comprises:

(a5) **reconfiguring** said link selection register at said source node to route said cell away from said intermediate node.

34. The method of claim 33 wherein step (a) further comprises:

(a2) detecting a **failed transaction** on said preferred path; and

(a3) retrying said failed transaction on a **non-preferred path.**

35. The method of claim 31 wherein said system interconnect includes an **intermediate node** and a **plurality of other nodes** each having a **node specific link selection register** and step (a) further comprises:

reconfiguring said node specific link selection register for each of said plurality of other nodes to select a **plurality of preferred paths** to every other of said plurality of other nodes, each of said plurality of preferred paths excluding said intermediate node.

36. A **method** for implementing a **system interconnect** for transporting a **cell** from a **source node** to a **destination node** on a **network** having a **plurality of rings**, each of said plurality of rings having a **plurality of nodes**, said plurality of rings including a **source ring** and a **second ring** with said source ring and said second ring connected by a **ring coupler node**, said method comprising steps of:

(a) **constructing** a **cell** having a **routing tag** having a **first forward hop address** and a **second forward hop addresses** by said source node;

(b) **transmitting** said cell onto said source ring;

(c) **swallowing** said cell from said source ring by said ring coupler node; and

(d) **transmitting** said cell onto said second ring by said ring coupler node.

37. The method of claim 36 wherein step (d) further comprises:

(d1) **replacing** said first forward hop address with said second forward hop address in said routing tag by said ring coupler node.

38. The method of claim 36 wherein step (d) further comprises:

(d1) **transmitting** a **response cell** corresponding to said cell back to said source node by said ring coupler node.

39. The method of claim 36 wherein step (d) further comprises:

(d1) **transmitting** a **response cell** corresponding to said cell back to said source node by said destination node.

40. A method for implementing a ring-to-ring coupler node with an **address** for transporting a **cell** comprising a **routing tag** from a **first ring** to a **second ring**, said method comprising steps of:

(a) **receiving** said cell from said first ring;

(b) **determining** disposition of said cell solely from said routing tag and said address; and

(c) **transmitting** said cell onto said second ring.

41. A **method** for recovering from loss of an **initial frequency reference signal** on a **first path** comprising steps of:

(a) **delaying** a **backup frequency reference signal** to generate a **delayed frequency reference signal** in phase with said initial frequency reference signal;

(b) **detecting** loss of said initial frequency reference signal; and

(c) **using** said delayed frequency reference signal.

42. The method of claim 41 wherein said backup frequency reference signal is a **master clock signal**, or a **frequency reference signal** on a **second path**.

43. A method for accessing a **first bus** connected to a **system interconnect** at a **first node** comprising steps of:

(a) **performing** a **bus operation** on a **second bus** connected to said system interconnect at a **second node**;

(b) **converting** said bus operation into a **cell**;

(c) **transporting** said cell over said system interconnect from said second node to said first node; and

(d) **performing** said an **equivalent bus operation** on said first bus by said first node after receipt of said cell by said first node.

44. The method of claim 43 wherein said first bus is a **first PCI bus** and said second bus is a **second PCI bus.**

45. The method of claim 43 further comprising:

(e) **obtaining** a **result** from performance of said equivalent bus operation on said first bus;

(f) **converting** said result into a **second cell**;

(g) **transporting** said second cell over said system interconnect from said first node to said second node; and

(h) **completing** said bus operation.

46. A **system interconnect apparatus** for transporting a **first cell** containing a plurality of **data** between a **plurality of nodes** wherein said system interconnect includes: **a first unidirectional path** between each **pair of adjacent nodes** of said plurality of nodes, said first unidirectional path includes an **incoming end** and an **outgoing end** and a **first plurality of signal lines** and a **frequency reference line**, said pair of adjacent nodes having a **source node** and a **receiver node**, said apparatus comprising:

a **clock originator node** configured to provide a **frequency reference signal** on said frequency reference line to said plurality of nodes;

a **phase lock loop frequency multiplier** configured to generate a **node clock** based on said frequency reference signal, said node clock having the same frequency for each of said plurality of nodes, said source node having a **source node clock** and said receiver node having a **receiver node clock**;

an **output section** of said source node connected to said outgoing end of an **output path** configured to transmit said first cell to said input section of said receiver node over a **first unidirectional path**, by emitting a plurality of **data transitions** using said source node clock, representing said first cell, onto a **first plurality of signal lines** at said outgoing end of said first unidirectional path; and

an **input section** of said receiver node connected to said incoming end of an **input path** configured to receive said data transitions using said receiver node clock, from said first plurality of signal lines at said incoming end of said first unidirectional path.

47. The apparatus of claim 46 wherein said first cell comprises a **destination address** and said receiver node further comprises a **node address** and a **routing decision logic mechanism** configured to compare said node address with said destination address.

48. The apparatus of claim 47 wherein said receiver node further comprises:

a **forwarding logic mechanism** configured to emit said plurality of data transitions, in synchronization with said receiver node clock, onto a **second plurality of data lines** at said outgoing end of a **second unidirectional path** while receiving said data transitions from said first plurality of signal lines, said forwarding logic mechanism dependent on said routing decision logic mechanism.

49. The apparatus of claim 47 wherein said receiver node further comprises:

an **emitting decision mechanism** configured to detect that said receiver node is transmitting a **second cell** at said outgoing end of a **second unidirectional path**;

a **bypass buffer** configured to store a **third cell** if said node address is different from said destination address, said third cell constructed from said data transitions received by said input section;

a **finished emitting decision mechanism** configured to detect when said second cell has been completely transmitted; and

a **transmit cell from bypass buffer mechanism** configured to transmit said third cell from said bypass buffer at said outgoing end of said second unidirectional path.

50. The apparatus of claim 47 wherein said receiver node further comprises:

a **cell swallowing mechanism** configured to swallow said plurality of data transitions defining a **second cell**, said cell swallowing mechanism dependent on said routing decision logic mechanism.

51. The apparatus of claim 50 wherein said receiver node further comprises:

a **cell management mechanism** configured to process said second cell; and

a **response cell mechanism** configured to transmit a **response cell** addressed to said source node from said output section of said receiver node.

52. The apparatus of claim 51 wherein said source node further comprises:

an **incomplete transaction cache** (ITC) configured to store a **copy of said first cell** in a **cell storage**, said ITC further configured to remove said copy of said first cell from said cell storage dependent on receipt of a response cell at said source node.

53. The apparatus of claim 47 wherein said first cell is a **broadcast cell** and said receiver node further comprises:

a **cell swallowing mechanism** configured to swallow said plurality of data transitions defining a **second cell**; and

a **forwarding logic mechanism** configured to emit said plurality of data transitions, in synchronization with said receiver node clock, onto a **second plurality of data lines** at said outgoing end of a **second unidirectional path** while receiving said data transitions from said first plurality of signal lines.

54. The apparatus of claim 53 wherein said receiver node further comprises:

a **cell processing mechanism** configured to process said second cell and to generate a **status**; and

a **response mechanism** configured to transmit a **response cell** to said source node, said response cell containing said status .

55. The apparatus of claim 46 wherein each node further comprises:

a **training signal generator** configured to emit a plurality of **training signal edges** on each of said first plurality of signal lines; and

an **initialization logic** configured to condition each of said plurality of DLLs such that said training signal edges received from said first plurality of signal lines at said incoming end of said first unidirectional path are synchronized with said node clock.

56. The apparatus of claim 46 wherein said input section comprises:

a plurality of **adjustable delays** with one adjustable delay for each of said first plurality of signal lines; and

a **synchronization mechanism** configured to synchronize said data transitions from said first plurality of signal lines to said receiver node clock through use of said plurality of adjustable delays.

57. The apparatus of claim 46 wherein said input section comprises:

an **adjustable delay**; and

a **synchronization mechanism** configured to synchronize said data transitions from said first plurality of signal lines to said receiver node clock through use of said adjustable delay.

58. A **system interconnect initialization apparatus** for initializing a **plurality of nodes** on a **ring network** having a **plurality of links**, said system comprising:

(a) a **first reset mechanism** configured to emit a **reset sequence** from a **first node** to reset a **second node** upon detection of said reset sequence;

(b) a **second reset mechanism** configured to emit said reset sequence from said second node; and

(c) a **reset termination mechanism** configured to terminate emission of said reset sequence by said first node upon receipt of said reset sequence at said first node.

59. The apparatus of claim 58 further comprising:

(d) a **first training mechanism** configured to emit a **training sequence** from said first node to train said second node;

(e) a **second training mechanism** configured to emit said training sequence from said second node; and

(f) a **training termination mechanism** configured to terminate emission of said training sequence by said first node upon receipt of said training sequence at said first node.

60. A **system interconnect apparatus** having a **plurality of nodes**, said apparatus for transporting a **cell** from a **source node** to a **destination node** on a **ring network** having a **first path** and a **second path**, one of said plurality of nodes being a **configuration node**, said apparatus comprising:

an **initialization mechanism** configured to initialize said plurality of nodes;

a **first emitting mechanism** in said configuration node configured to emit a **first identifying address sequence** containing a **configuration node address** onto said first path;

a **first receiving mechanism** in a **second node** configured to receive from said first path said first identifying address sequence;

an **address modification mechanism** configured to modify said configuration node address contained in said first identifying address sequence to create a **second node address**; and

a **second emitting mechanism** in said second node configured to emit onto said first path a **second identifying address sequence** containing said second node address.

61. The apparatus of claim 60 further comprising:

a **third emitting mechanism** in said configuration node configured to emit said first identifying address sequence containing said configuration node address onto said second path;

a **second receiving mechanism** in said second node configured to receive from said second path a **third identifying address sequence** dependent on said second node's position on said second path;

a **node number determination mechanism** in said second node configured to determine a **number of nodes** on said ring network using said second identifying address sequence and third identifying address sequence; and

a **link selection register initialization mechanism** configured to initialize a **link selection register** (LSR) to indicate which of said first path and said second path is a **preferred path** to each of said plurality of nodes by using information contained in said first identifying address sequence and said third identifying address sequence.

62. A **system interconnect apparatus** for transporting a **cell** from a **source node** on a **ring network** to a **destination node** on said network, said network having a **plurality of links**, said apparatus comprising:

an **interrupt detection mechanism** configured to detect an **interrupt condition change** at said source node, said interrupt condition change comprising either an **interrupt assertion** or an **interrupt deassertion**;

an **interrupt cell creation mechanism** configured to create an **interrupt cell** at said source node responsive to the interrupt detection mechanism, said interrupt cell being addressed to said destination node and containing said interrupt condition change;

a **cell transportation mechanism** configured to transport said interrupt cell to said destination node; and

an **interrupt assertion mechanism** configured to assert an **interrupt signal** at said destination node responsive to said interrupt condition change.

63. The apparatus of claim 62 wherein the interrupt assertion mechanism further comprises:

an **interrupt assertion recognition mechanism** at said destination node configured to recognize said interrupt cell containing said interrupt assertion and increment an **up/down counter**.

64. The apparatus of claim 63 wherein the interrupt assertion mechanism further comprises:

a **post interrupt mechanism** configured to detect that said up/down counter is non-zero and to post an **interrupt** at said destination node.

65. The apparatus of claim 62 wherein said cell further comprises a **source node identifier** and the interrupt assertion mechanism further comprises:

a **storage mechanism** configured to save said source node identifier and said interrupt condition change.

66. The apparatus of claim 62 wherein the interrupt assertion mechanism further comprises:

an **interrupt deassertion recognition mechanism** at said destination node configured to recognize said interrupt cell containing said interrupt deassertion; and decrement an **up/down counter**.

67. The apparatus of claim 66 wherein the interrupt assertion mechanism further comprises:

a **clear interrupt mechanism** configured to detect that said up/down counter is zero and to clear an interrupt at said destination node.

68. The apparatus of claim 62 wherein said interrupt cell comprises an **interrupt security code** and the interrupt assertion mechanism further comprises:

an **interrupt security mechanism** configured to match said interrupt security code with a **destination node interrupt security code**.

69. A **system interconnect apparatus** for transporting a **cell** from a **source node** to a **destination node** on a **ring network** having a **plurality of destination nodes**, said network having a **plurality of links**, said apparatus comprising:

an **incomplete transaction cache** configured to track a **number of incomplete transactions**;

a **delay mechanism** configured to delay generation of said cell if one more than said number of incomplete transactions is outside a **sliding window width**;

a **cell generation mechanism** configured to **generate** said cell after one more than said number of incomplete transactions is within said sliding window width; and

a **cell transport mechanism** configured to transport said cell to said destination node.

70. The apparatus of claim 69 wherein the incomplete transaction cache further comprises a **node specific tracking mechanism** configured to track one of said number of transactions sent from said source node to said destination node.

71. The apparatus of claim 69 wherein said apparatus further comprises:

an **first accounting mechanism** configured to account for an **increase** in said number of incomplete transactions.

72. The apparatus of claim 71 wherein said apparatus further comprises:

a **response cell detection mechanism** configured to detect a **response cell** sent from said destination node;

a **transaction completion mechanism** configured to complete an **incomplete transaction** dependent on said response cell; and

a **second accounting mechanism** configured to account for a **decrease** in said number of incomplete transactions.

73. The apparatus of claim 69 wherein said destination node is a **hop node.**

74. The apparatus of claim 69 wherein the incomplete transaction cache further comprises:

a **receiving mechanism** configured to receive, by said source node, a **previously sent cell** sent from said source node and to reduce a **sliding window width.**

75. The apparatus of claim 69 wherein the incomplete transaction cache further comprises:

a **tracking mechanism** configured to track a **plurality of number of incomplete transactions** sent from said source node to each of said plurality of destination nodes.

76. A **system interconnect apparatus** for transporting a **cell** from a **source node** to a **destination node** on a **ring network** wherein said network includes a **clockwise path** and a **counterclockwise path**, said apparatus comprising:

a **link selection register access mechanism** configured to access a **link selection register** at said source node to select which of said clockwise path and said counterclockwise path transports said cell; and

a **cell transport mechanism** configured to **transport** said cell to said destination node over said clockwise or counterclockwise path as selected.

77. The apparatus of claim 76 wherein the link selection register access mechanism further comprises:

an **initialization mechanism** configured to initialize said link selection register at said source node to specify a **preferred path** to said destination node by specifying which of said clockwise path and said counterclockwise path is used to transport said cell to said destination node.

78. The apparatus of claim 77 wherein the system interconnect includes an **intermediate node** between said source node and said destination node on one of said paths, and the link selection register access mechanism further comprises:

a **reconfiguration mechanism** configured to reconfigure said link selection register at said source node to route said cell away from said intermediate node.

79. The apparatus of claim 78 wherein the link selection register access mechanism further comprises:

a **failure detection mechanism** configured to detect a **failed transaction** on said preferred path; and

a **recovery mechanism** configured to retry said failed transaction on a **non-preferred path**.

80. The apparatus of claim 76 wherein said system interconnect includes an **intermediate node** and a **plurality of other nodes** each having a **node specific link selection register** and the **link selection register access mechanism** further comprises:

a **link selection register modification mechanism** configured to **modify** said node specific link selection register for each of said plurality of other nodes to select a **plurality of preferred paths** to every other of said plurality of other nodes, each of said plurality of preferred paths excluding said intermediate node.

81. A **system interconnect apparatus** for transporting a **cell** from a **source node** to a **destination node** on a **network** having a **plurality of rings**, each of said plurality of rings having a **plurality of nodes**, said plurality of rings including a **source ring** and a **second ring** with said source ring and said second ring connected by a **ring coupler node**, said apparatus comprising:

a **cell construction mechanism** in said source node configured to construct a **cell** with a **routing tag** having a **first forward hop address** and a **second forward hop addresses**;

a **first transmission mechanism** in said source node configured to transmit said cell onto said source ring;

a **swallowing mechanism** in said ring coupler node configured to swallow said cell from said source ring; and

a **second transmission mechanism** in said ring coupler node configured to transmit said cell onto said second ring.

82. The apparatus of claim 81 wherein the second transmission mechanism further comprises:

a **hop update mechanism** configured to replace said first forward hop address with said second forward hop address in said routing tag by said ring coupler node.

83. The apparatus of claim 81 wherein the second transmission mechanism further comprises:

a **response mechanism** configured to transmit a **response cell** corresponding to said cell back to said source node by said ring coupler node.

84. The apparatus of claim 81 wherein the second transmission mechanism further comprises:

a **response mechanism** configured to transmit a **response cell** corresponding to said cell back to said source node by said destination node.

85. A **ring-to-ring coupler node apparatus** with an **address** for transporting a **cell** from a **first ring** to a **second ring**, said cell comprising a **routing tag**, and said apparatus comprising:

a **cell receiving mechanism** configured to receive said cell from said first ring;

a **cell disposition mechanism** configured to determine disposition of said cell solely from said routing tag and said address; and

a **cell transmission mechanism** configured to transmit said cell onto said second ring.

86. An **apparatus** for recovering from loss of an **initial frequency reference signal** on a **first path** comprising:

a **delay mechanism** configured to delay a **backup frequency reference signal** to generate a **delayed frequency reference signal** in phase with said initial frequency reference signal;

a **detector mechanism** configured to detect loss of said initial frequency reference signal on said first path; and

a **switch mechanism** configured to emit said delayed frequency reference signal on said first path.

87. The apparatus of claim 86 wherein said backup frequency reference signal is a **master clock signal**, or a **frequency reference signal** on a **second path**.

88. An apparatus for accessing a **first bus** connected to a **system interconnect** at a **first node** comprising:

a **bus capture mechanism** at a **second node** configured to capture a **bus operation** on a **second bus** connected to said system interconnect;

a **first cell generation mechanism** at said second node configured to convert said bus operation into a **cell**;

a **first cell transportation mechanism** configured to transport said cell over said system interconnect from said second node to said first node; and

a **bus operation mechanism** at said first node configured to perform an **equivalent bus operation** on said first bus after receipt of said cell by said first node.

89. The apparatus of claim 88 wherein said first bus is a **first PCI bus** and said second bus is a **second PCI bus**.

90. The apparatus of claim 88 further comprising:

a **result acquisition mechanism** at said first node configured to obtain a **result** from performance of said equivalent bus operation on said first bus;

a **second cell generation mechanism** at said first node configured to convert said result into a **second cell**;

a **second cell transportation mechanism** at said first node configured to transmit said second cell over said system interconnect from said first node to said second node; and

a **bus operation completion mechanism** at said second node configured to complete said bus operation.

91. A method for automatically constructing a **routing tag** for a **cell** based on an **address** provided by a **bus operation** on a bus connected to a **first node** of a **system interconnect** comprising the steps of:

(a) **capturing** said address from said bus; and

(b) **converting** said address into a **value** stored in said routing tag.

92. The method of claim 91 wherein step (b) further comprises:

(b1) **accessing** said value from a **first address mapping content addressable memory** (fAMCAM) after assertion of said address to said fAMCAM.

93. The method of claim 92 wherein said fAMCAM comprises a **first register** that defines an **address window** on said bus.

94. The method of claim 93 wherein said system interconnect further comprises a **second node** with a **second address mapping content addressable memory** (sAMCAM) and a **second register**, and said method further comprises:

(c) **storing** a **configuration value** in said first register; and

(d) **broadcasting** said configuration value to said second node for storage in said second register.

95. An apparatus for automatically constructing a **routing tag** for a **cell** based on an **address** provided by a **bus operation** on a bus connected to a **first node** of a **system interconnect** comprising:

an **address capturing mechanism** configured to capture said address from said bus; and

an **address conversion mechanism** configured to convert said address from said bus into a **value** stored in said routing tag of said cell.

96. The apparatus of claim 95 wherein the address conversion mechanism further comprises:

a **first address mapping content addressable memory** (fAMCAM) configured to produce said **value** after assertion of said address to said fAMCAM.

97. The apparatus of claim 96 wherein said fAMCAM comprises a **first register** that defines an **address window** on said bus.

98. The apparatus of claim 97 wherein said system interconnect further comprises a **second node** with a **second address mapping content addressable memory** (sAMCAM) and a **second register** and said apparatus further comprises:

a **storage mechanism** configured to store a **configuration value** in said first register; and

a **broadcast mechanism** configured to broadcast said configuration value to said second node for storage in said second register.